1. Changes to CHRP binding for Version 1.8

1.1. Open PIC, Section 5.5.1 (Open PIC Interrupt Controller Nodes)

Add a new section, under Section 5.5, Interrupt Controller Nodes.

3.1.6.1. Bootinfo Entities

Remove "\" from definition of the fully qualified pathname as specified in proposal #419.

5.5.2. Open PIC Interrupt Controller Child Node Properties

An *open-pic* child node is defined to be a child of the Open PIC Controller or an interrupt source that connects to the Open PIC Interrupt Controller.

`"interrupts"` **`S`**

Standard *property name*, the presence of which indicates that the function or source represented by this node is connected to an OpenPIC Interrupt Controller.

prop-encoded-array: list of an arbitrary number of integer pairs (*irq# type*) where:

irq# is an integer, encoded as with **`encode-int`**. The *irq#* integer represents the interrupt line to which this function's interrupt is connected. This value is in the range 0..2047 (decimal).

type is an integer, encoded as with **`encode-int`**, indicating an interrupt type. The interrupt types are represented by the following integer values:

0 = low to high edge sensitive type enabled

1 = active low level sensitive type enabled

Refer to *Recommended Practice - Interrupt Mapping* [15] for Open Firmware interrupt structure.

Note: For an MPIC implementation, a `"compatible"` property should be present with the following value:

compatible = `"pci,1014,46"`

Open Firmware should set the MPIC 'polarity' and 'sense' bits from the following table for the correct system state:

Table 1. MPIC 'polarity' and 'sense' bit states

Polarity	Sense	MPIC State
0	0	negative edge (**Note 1**)
0	1	active low (**Note 2**)
1	0	positive edge (**Note 1**)
1	1	active high

Note 1: State should not be used because 'Edge' mode does not work for MPIC Part

Note 2: State should not be used for source 0 because of passthrough mode

Work Item: Need to find place/mechanism in documentation to put note about MPIC Implementation. Apple's version of MPIC in the Hydra Chip works with edge mode interrupts (Note 1 above in Table 1).